A 1-Watt Flyback Converter Using the Si9100

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The Si9100 is a monolithic BiC/DMOS SMARTPOWER IC which combines high-efficiency CMOS logic, a high-voltage switching transistor and high-voltage pre-regulator on a single die. It is the first low-cost, high efficiency regulator designed to operate directly from unregulated high-voltage dc power sources in areas such as telecommunications and avionics. The primary application will be in feature phones and ISDN terminals to power the logic components without exceeding the load limits set by the telecommunications industry. Power integrated circuit technology allows low-power CMOS control circuits to be combined with DMOS power transistors in the Si9100. The resulting reduced parts count decreases system cost, improves reliability, and simplifies circuit design.

The flyback converter presented here uses the Si9100 to provide an isolated ±5 V supply rated at 1 W. Specifications for this supply are as follows:

Input Voltage	15 to 70 V_{DC}
Maximum load	+5 V @ 167 mA,
	−5 V @ 33 mA
Minimum load	+5 V @ 32 mA,
	−5 V @ 8 mA
Regulation	±5%
Maximum Ripple	100 mV p-p
Switching Frequency . .	100 kHz
Efficiency	80% min for 1 W load
	75% min for 0.2 W load

A schematic for the flyback converter is found in Figure 1, with a parts list provided in Appendix B. However, before discussing the details of the power supply design, it is instructive to review the functions of the Si9100 integrated circuit.

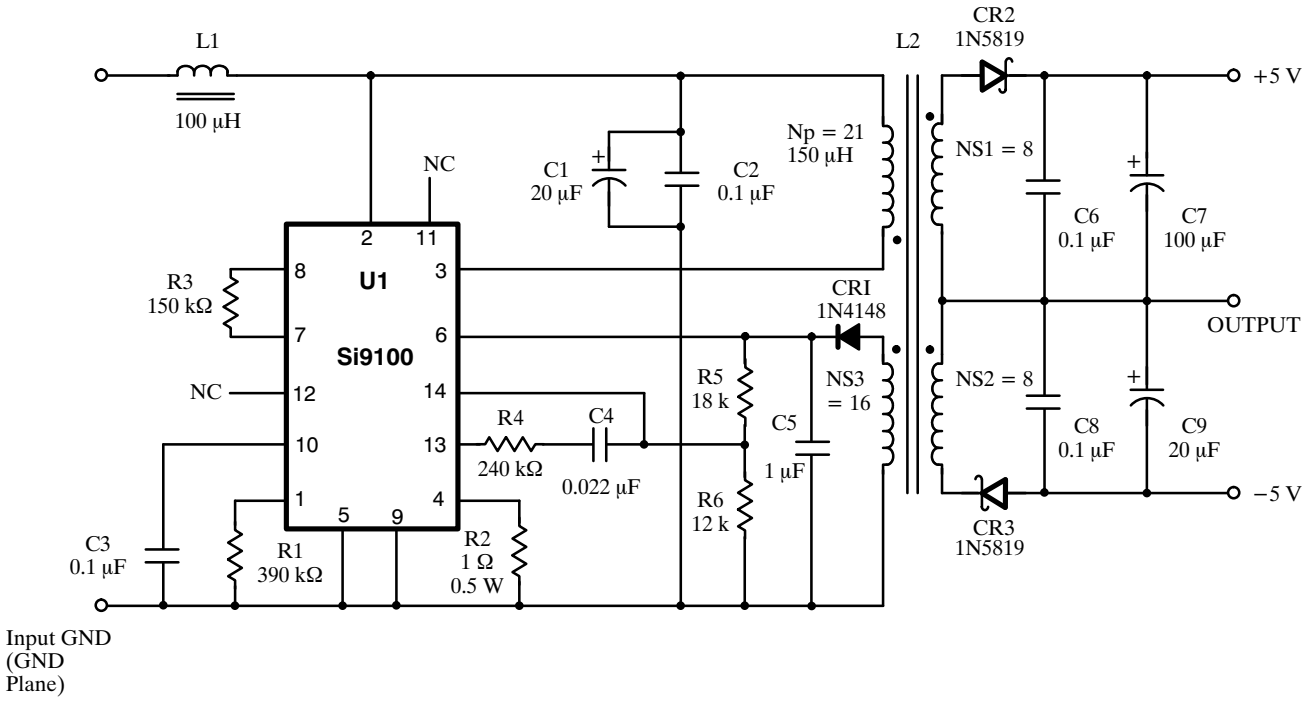

Figure 1. Schematic Diagram of the Si9100 Discontinuous Flyback Converter Circuit

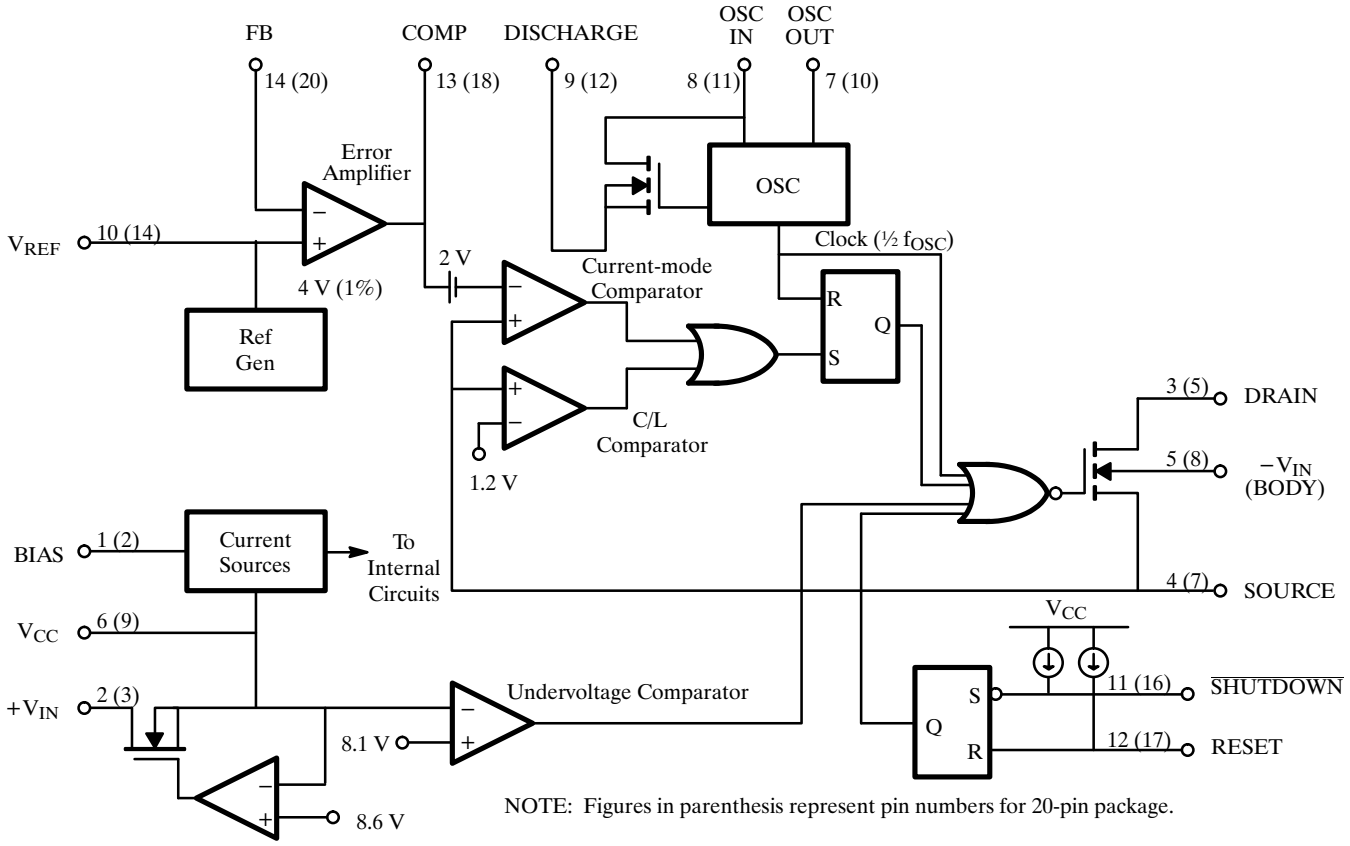

Figure 2. Si9100 Simplified Block Diagram

Si9100 Description

As shown in the block diagram of Figure 2, the Si9100 combines an oscillator, pre-regulator/start-up circuit, precision voltage reference, error amplifier, current-mode controller, and a MOSFET switching transistor into one 14-pin dual-in-line package. Overcurrent protection, undervoltage lockout, and logic inputs for both latched and unlatched shutdown modes are also included.

Start-up/Preregulator Circuit

A unique start-up/preregulator circuit, which is shown in Figure 3, permits the Si9100 to operate over a wide input voltage range (10 to 70 V). The input voltage for the device is connected between the $+V_{IN}$ (pin 2) and $-V_{IN}$ (pin 5) terminals. The high-voltage depletion-mode (normally ON) MOSFET acts as a current source during start-up, charging the capacitance at the V_{CC} terminal (pin 6) directly from the input source. When V_{CC} exceeds the 8.1 V undervoltage threshold, the output switch is enabled to provide well-defined start-up characteristics. V_{CC} is then regulated to 8.6 V by the pre-regulator circuit. If an external voltage source greater than 8.6 V is fed to the V_{CC} terminal, the depletion-mode MOSFET is shut off to reduce power drain from the input power source.

Oscillator

The oscillator requires a single resistor to set its frequency. The requirements of flux reset in single-ended converters generally dictates a maximum duty cycle of 50%. With the oscillator frequency set at two times the desired switching frequency, a flip-flop divides the clock signal by two, and the logic disables the output during every other clock cycle.

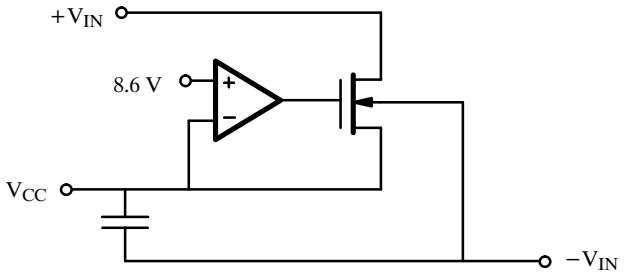

Figure 3. Schematic Diagram of the Start-up Section of the Si9100

MOSFET Switch

The MOSFET switching transistor has typical $r_{DS(ON)}$ and $V_{(BR)DSS}$ characteristics of 4 Ω and 180 V, respectively. Worst case specifications are 5 Ω and 150 V. The device is a lateral DMOS structure which has external connections for the DRAIN (pin 3) and SOURCE (pin 4). The body of the MOSFET is internally tied to the $-V_{IN}$ terminal, which must be connected to the most negative input potential in the circuit.

Error Amplifier

The error amplifier permits compensation of control loops for stable regulator operation. The amplifier uses PMOS input transistors to provide high input impedance (2 MΩ minimum), and is internally compensated for unity gain stability, with 1 MHz (typical) bandwidth and 60° phase margin.

Protection

In addition to the undervoltage lockout function already described, the Si9100 provides overcurrent protection and inputs for external logic control. With a sense resistor (typically 1 to 2 Ω) connected from the MOSFET source to the $-V_{IN}$ terminal, the voltage at pin 4 is proportional to the output current. When this voltage exceeds a 1.2 V reference the overcurrent comparator disables the output MOSFET. The shutdown delay is typically 100 ns (200 ns maximum).

Logic inputs $\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) permit the use of latched or unlatched shutdown modes. Internal current source pull-ups normally hold both logic pins high. If the $\overline{\text{SHUTDOWN}}$ pin is pulled low while the RESET is high, then the output switch will be disabled until the $\overline{\text{SHUTDOWN}}$ pin is again allowed to go high. This is the unlatched shutdown mode. If, however, the RESET pin is pulled low while the $\overline{\text{SHUTDOWN}}$ pin is also pulled low, then the converter will be latched off until RESET goes high again.

Flyback Converter Operation

Start-up

Applying input voltage to the circuit initiates charging of capacitor, C_1, through the filter inductor, L_1. The depletion-mode MOSFET, as described above, supplies current to capacitor C_5 through the V_{CC} terminal of the IC. When V_{CC} reaches the undervoltage threshold (8.1 V), then transistor switching begins. The 4 V reference and the voltage divider ratio formed by R_5 and R_6 cause the feedback winding, N_{S3}, to be regulated to +10 V. After start-up is complete the feedback voltage trips the comparator to turn off the pre-regulator circuit, and the Si9100 derives its bias power from the feedback winding. The power saved by this bootstrap technique is equal to the product of the IC supply current times the difference between V_{IN} and V_{FB}:

Power Saved = (600 μA) (48 V − 10 V) = 23 mW

While this is not a great deal of power, it does represent 2.3% of the output for a 1 W supply. Integrated Services Digital Network (ISDN) applications require such techniques for bias power minimization in order to meet emergency-mode limits for the power-down state.

Flyback Operation

Flyback converter operation is illustrated by the basic waveforms shown in Figure 4. When the MOSFET switch is turned on, current will ramp up in the primary at a rate given by:

$$\frac{di}{dt} = \frac{V}{L} = \frac{I_{pk}}{t_{ON}}$$

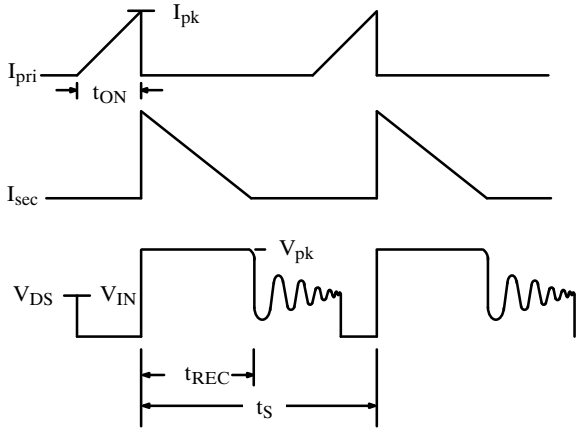

Figure 4. Flyback converter waveforms

Stored energy, given by ½ L_P I_{pk}^2, is present in L_2 at the time the MOSFET is switched off. This energy is released to the secondary windings, N_{S1} through N_{S3}, during the off time, as shown by the total secondary current, I_{sec}, in Figure 4.

This is the flyback principle in its simplest terms. A transformer is designed to transfer energy directly from the primary to the secondary, with as little stored energy as possible.

A flyback inductor receives energy during one interval of the switching cycle, then releases this stored energy at a later interval of the switching cycle.

During the time that the secondaries are conducting, shown as t_{REC}, the magnetic flux recovers, or "resets" to zero, and the MOSFET must block the sum of the reflected voltage from the secondary and the input voltage. This requires a worst case blocking voltage of:

$$V_{pk} = V_{IN} + \frac{N_P}{N_{S1}} (V_O + V_D)$$

$$= 70 + \frac{21}{8} (5.0 + 0.5) = 85 \text{ V}$$

A leakage inductance spike appears at the leading edge of the V_{DS} waveform. The spike is less than the 150 V minimum $V_{(BR)DSS}$, and no snubber network is required. Since the flux is reset to zero before the end of each switching cycle, current flow through the secondary is discontinuous. Consequently, this circuit is called a discontinuous-conduction-mode (DCM) flyback converter.

Regulator Control Loop

The function of the regulator control loop is to maintain the output voltages constant as either the input line voltage or load current vary. These are termed "line regulation" and "load regulation", respectively.

A sense winding has been chosen to close the regulator loop and provide output isolation. Since the secondary windings are coupled on a common core, the volts/turn ratio is the same for N_{S1}, N_{S2} and N_{S3}. The resulting secondary voltages will track each other quite closely. There is, however, some degradation in load regulation due to leakage (uncoupled) inductance between the ±5 V output windings and the sense winding. This effect becomes progressively worse as the switching frequency is increased. The coupled inductor used here has been designed for good coupling between output and sense windings in order to maintain better than 5% regulation over the 0.2 W to 1 W load range. Design details for the coupled inductor are included in Appendix A.

To analyze the system closed loop response, begin by reflecting the filter capacitance and load resistance from each output winding to the feedback winding.

$$C_{eff} = C_5 + \left(\frac{N_{S1}}{N_{S3}}\right)^2 \bullet \left(C_7 + C_9\right)$$

$$= 1 \text{ µF} + \left(\frac{8}{16}\right)^2 (100 \text{ µF} + 20 \text{ µF}) = 31 \text{ µF}$$

The effective load resistance, R_{eff}, can be found by assuming that the entire 1 W load is connected across the sense winding output:

$$R_{eff} = \frac{V_S^2}{P_O} = \frac{(10 \text{ V})^2}{1 \text{ W}} = 100 \text{ Ω}$$

The effective load impedance is determined at low frequency by the 100 Ω resistance and at high frequency by the capacitive reactance given by $X_C = 1/\omega C_{eff}$. The control-to-output transfer function thus has a pole at:

$$f_p = \frac{1}{2\pi R_{eff} C_{eff}} = \frac{1}{2\pi (100) (31 \text{ S } 10^{-6})} = 51 \text{ Hz}$$

To calculate the low frequency gain of the power stage, assume a 1 mV change in the error voltage, V_e, at the output of the error amplifier, and calculate the voltage change, ΔV_S, which results at the feedback winding. Then combine the power stage gain with the error amplifier gain (including the voltage divider) to yield the total loop response. Assume for these calculations that the converter efficiency remains constant at 83.33%.

$$P_{IN} = \frac{P_O}{\eta} = \frac{1 \text{ W}}{0.8333} = 1.2 \text{ W}$$

The power input to the converter is the product of the stored inductive energy times the switching frequency.

$$P_{IN} = ½ L_p (I_{pk})^2 \bullet f_s$$

Rearranging to solve for I_{pk} gives:

$$I_{pk} = \sqrt{\frac{2 P_{IN}}{L_P \bullet f_s}} = \sqrt{\frac{2 (1.2)}{(150 \text{ µH}) 10^5}} = 0.4 \text{ A}$$

Since the current sense resistor, R_2, equals 1 Ω, a 1 mV change in the error voltage (at pin 13) will result in a 1 mA change in the peak inductor current, i.e., $\Delta I_{pk} = \Delta V_e$. A 1 mA increase in I_{pk} causes P_{IN} to increase to:

$$P_{IN} = ½ L_p (I_{pk} + DI_{pk})^2 \bullet f_s =$$

$$½ \bullet 150 \bullet 10^{-6} (0.400 + 0.001)^2 \bullet 10^5 = 1.206 \text{ W}$$

Assuming efficiency remains constant,

$$P_O = (0.833) \bullet P_{IN} = 1.005 \text{ W}$$

This translates to an increase in the sense voltage to:

$$V_S = \sqrt{P_O \bullet R_{eff}} = \sqrt{(100 \bullet 1.005)} = 10.025 \text{ V}$$

The gain is given by:

$$\frac{\Delta V_S}{\Delta V_e} = \frac{10.025 \text{ V} - 10 \text{ V}}{1 \text{ mV}} = 25$$

At full load the low frequency gain of the power stage is 25 (28 dB), with a single pole in the transfer function at 51 Hz. Performing a similar calculation at the 20% load condition yields a gain of 56 (35 dB) with a pole at 10 Hz. There will also be a zero in the transfer function at approximately 30 kHz due to capacitor ESR.

The solid line in Figure 5 represents the transfer function of the converter power stage at full load. The corresponding curve at a 20% load is shown in Figure 6. To complete the analysis of the control loop requires accounting for the resistive voltage divider and the error amplifier. The resistor R_6 sets the dc bias condition, but does not enter into the samll signal analysis.

At high frequencies the gain is R_4/R_5, with a zero occurring in the transfer function at

$$f_z = \frac{1}{2\,\pi\,(240\ \text{k}\Omega)\,(0.022\ \mu\text{F})} = 30 \text{ Hz}$$

The error amplifier response is shown in Figures 5 and 6 as dashed lines. The error amplifier response times the power stage gain gives the total loop gain, which is shown as the gray line for full load in Figure 5 and light load in Figure 6. Actual measurements of loop gain and phase yielded a loop bandwidth of 14 kHz with 68 degrees phase margin. Figure 7 shows the response of the +5 V output as the load is stepped between 20% and 100% of full load. Response time is under 200 µs with no overshoot.

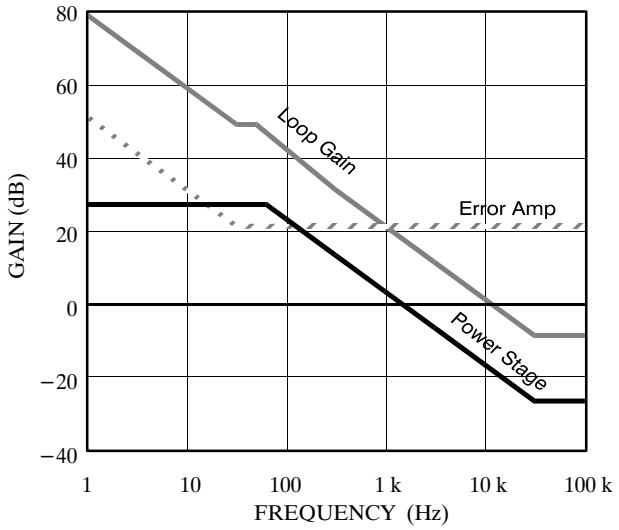

Figure 5. Loop gain at 100% load

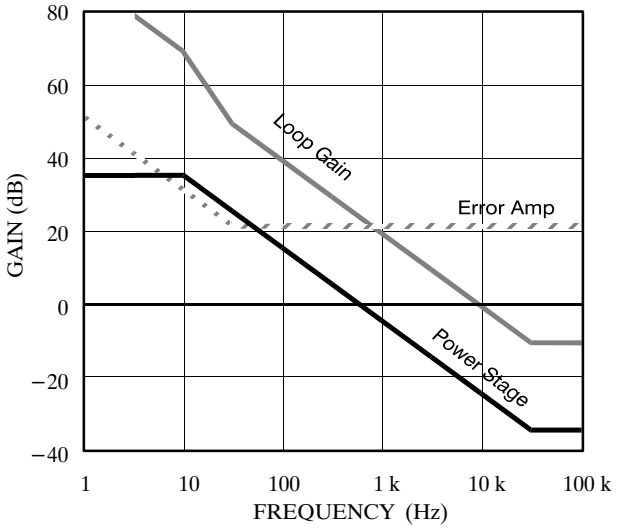

Figure 6. Loop gain at 20% load

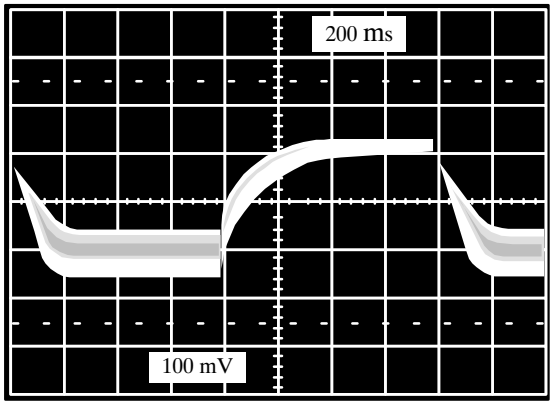

Figure 7. Step Load Response

ISDN APPLICATIONS

Integrated Services Digital Network (ISDN) poses some unique problems to telecom systems design engineers. Standards proposed by the International Telephone and Telegraph Consultative Committee (CCITT) recommend that input power to ISDN terminal equipment (TE) meet the limits outlined in Table I[1].

Table I. ISDN Power Requirements

Operating Mode	Maximum Input Power to TE	Efficiency Target
Normal-active	900 mW	70%
Normal-power down	100 mW	60%
Emergency-active	400 mW	70%
Emergency-power down	25 mW	40%

The 25 mW limit during emergency power-down mode operation may be especially troublesome[2]. In order to supply 10 mW to the TE for such functions as memory back-up, total converter losses must be less than 15 mW. Under such light load conditions the major power loss is in the PWM controller. Only controllers implemented in CMOS can presently be expected to meet this requirement.

Although the converter circuit of Figure 1 was not designed specifically for use in ISDN terminals, with some modifications it can be used in these applications. Since CMOS logic circuits consume power only during switching transitions, the first modification which is recommended is to decrease the switching frequency. The coupled inductor, L_2, can be operated at 40 to 50 kHz (change R_3 from 150 kΩ to 390 kΩ) without a redesign. Decreasing the frequency further requires a larger core size.

A second circuit modification which is recommended is to increase the resistances used in the voltage divider network (R_5 and R_6). The values used in the 1 W converter will dissipate $(10)^2/(18\ k\Omega + 12\ k\Omega) = 3.33$ mW. This loss is negligible for the 1 W converter, but it is nearly one fourth of the budgeted power loss for the ISDN supply during the emergency power-down state. Setting $R_5 = 51.1$ kΩ and $R_6 = 34.0$ kΩ reduces the voltage divider dissipation to 1.2 mW. With these two minor changes the flyback converter meets the efficiency specifications of Table I. Figure 8 illustrates the efficiency improvement at light load levels which results from the circuit changes outlined above.

Other Si9100 Applications Circuits

The Si9100 has been called a “One Watt High-Voltage Switchmode Regulator” in order to describe its most appropriate type of application--low power converters. The device is not, however, limited to 1 W designs. Figure 9 shows the maximum achievable output power as a function of minimum input voltage for several types of converters, two of which are discussed below.

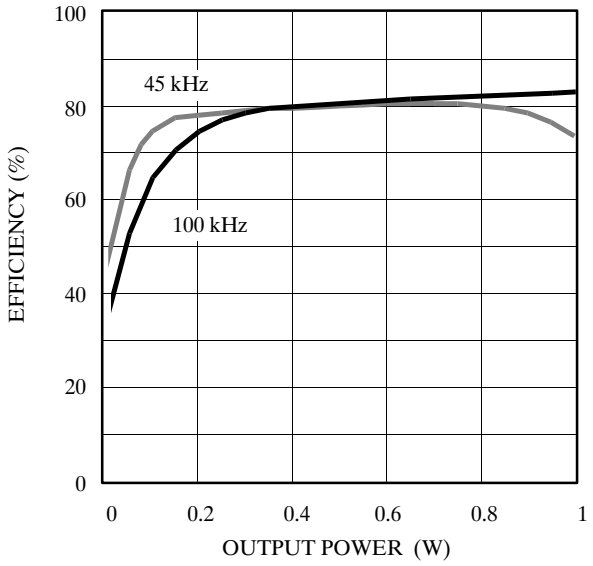

Figure 8. Efficiency vs. load curves for the flyback converter

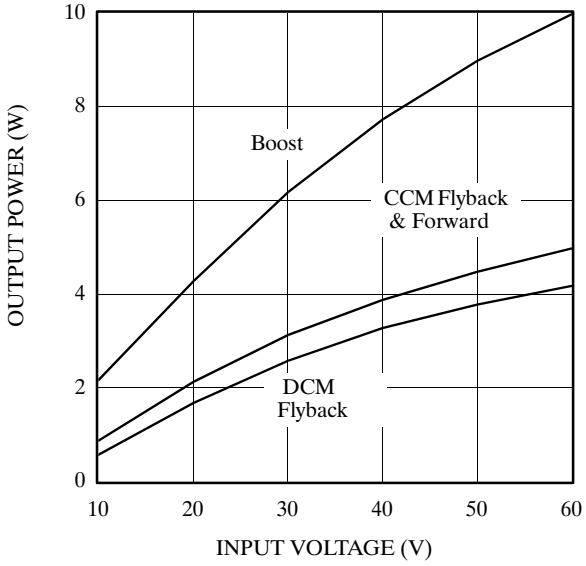

Figure 9. Maximum output power vs. minimum input voltage

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CCM Flyback Converter

By redesigning the magnetics for continuous conduction, the flyback circuit of Figure 1 can be made to provide 3 W of output power. Operation in the continuous conduction mode (CCM) introduces a right-half-plane (RHP) zero into the control-to-output transfer function of the power stage. The RHP zero incurs a phase lag without the corresponding gain rolloff caused by left-half-plane poles, and lead compensation cannot be used. Instead, the gain must be rolled off to unity (0 dB) below the RHP zero frequency. The continuous-mode flyback will, therefore, have a slower dynamic response than the DCM flyback. Also, to maintain the same output ripple for the 3 W converter, it is necessary to increase the size of the output filter capacitors.

Forward Converter

Forward converters are not normally used for power supplies rated under 50 W, due to the additional cost of the output filter chokes. However, for 2 to 4 W converter applications requiring ultra-low ripple, the cost of the additional inductor may be warranted. One such application is low power instrumentation for avionics.

The forward converter of Figure 10 was designed to operate from 28 V aircraft power (MIL-STD-704D) to provide 2.5 W at 80% efficiency.

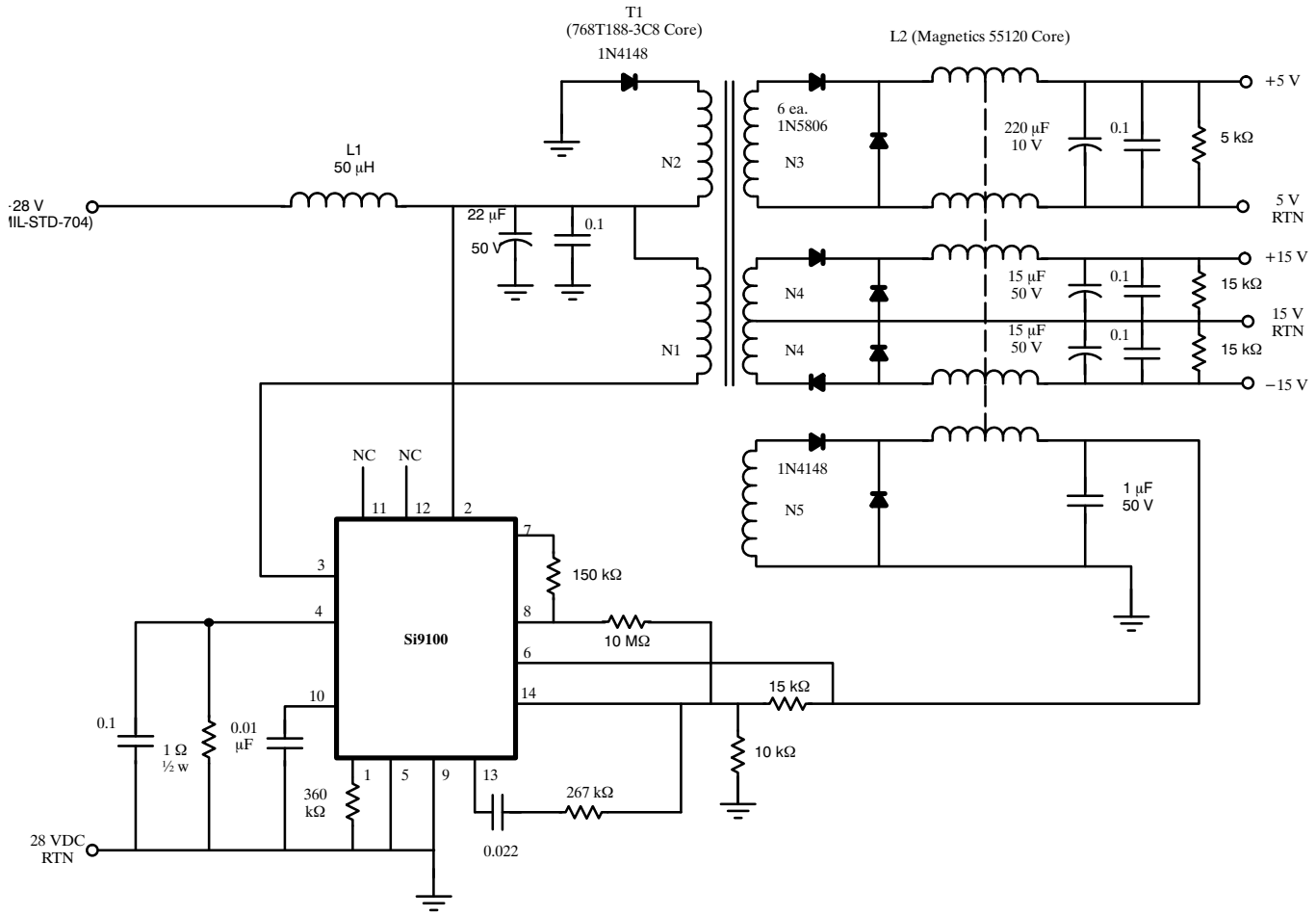

Figure 10. 2.5 W Forward Converter Using the Si9100

A single core with multiple windings has been used to decrease cost and board space required for the output filter inductors. The input voltage range is 18 to 32 V_{DC}; regulation is 5%; and the switching frequency is 100 kHz. Measured peak-to-peak voltage ripple was 8 mV for the +15 V output, 4 mV for the −15 V output, and 13 mV for the +5 V output, at maximum load.

Toroidal cores were used for both the transformer and the coupled output inductor to achieve very low leakage inductance. The transformer winding data is as follows:

Core - Ferroxcube #768T188-3C8

Windings - N1 = 31 turns (AWG26)
N2 = 31 turns (AWG34)
N3 = 22 turns (AWG32)
N4 = 64 turns (AWG32)
N5 = 43 turns (AWG34)

The primary and clamp windings are placed on the core first, wound bifilar to minimize leakage inductance. The +5 V output is wound next, followed by the ±15 V outputs wound bifilar. The 10 V winding was placed on the outside. Each winding is spread over the entire circumference of the toroidal core for optimum magnetic coupling.

Coupled inductors must have the same turns ratios as the transformer secondaries or high circulating currents result in very high output ripple. The coupled inductor, L_2, is a molypermalloy powder (MPP) toroid (Magnetics #55120) with three times the number of turns as each of the T1 secondaries.The inductor winding data is as follows:

+5 V − 66 turns (AWG30)
+15 V − 192 turns (AWG30)
−15 V − 192 turns (AWG34)
+10 V − 129 turns (AWG34)

It should be mentioned here that MIL-STD-461 EMI testing was not performed for this supply. To meet CE03 and CS01 limits, some input filter redesign is required. Although current-mode control exhibits excellent audio-susceptibility performance, it is still necessary to damp the input filter to reduce peaking of its output impedance at the resonant frequency (Reference 3 provides useful design information regarding these requirements).

References

1) Rosenbaum, D. and Stolp, K. H., “The Feeding Conception of the ISDN Basic Access,” IEEE Intelec Conference, Munich, FRG, Oct 14-17, 1985, pp. 505-512.

2) Krautkramer, W. and Schickling, B., “Remote Power Feeding of ISDN Terminals at the Basic Access,” IEEE Intelec Conference, Munich, FRG, Oct 14-17,1985, pp. 513-519.

3) Middlebrook, R. D., “Input Filter Considerations in Design and Application of Switching Regulators,” IEEE Industry Applications Society Annual Meeting, Oct. 11-14, 1976.

Appendix A: Flyback Inductor Design

Inductance Calculation

The first step is to calculate the maximum primary inductance for discontinuous conduction at maximum load. Input power to the coupled inductor is approximately:

$$P_{IN} = \frac{1\ W}{0.8} = 1.25\ W \qquad (1)$$

Input power is also equal to the product of the stored energy in the magnetic field times the switching frequency:

$$P_{IN} = \tfrac{1}{2}\, L_P\, (I_{pk})^2 \bullet f_s \qquad (2)$$

The minimum primary current slope occurs at the minimum input voltage condition.

$$\left.\frac{di}{dt}\right|_{MIN} = \frac{V_{IN(MIN)}}{L_{P(MAX)}}$$

If a maximum duty ratio of 0.45 is assumed, then the minimum current peak is given by:

$$I_{pk} \leq \left.\frac{di}{dt}\right|_{MIN} \bullet 0.45\ T_S$$

or

$$I_{pk} \leq \frac{V_{IN(MIN)}}{L_{P(MAX)}} \bullet 0.45\ T_S \qquad (3)$$

Combining equations 2 and 3 gives:

$$P_{IN(MAX)} = \tfrac{1}{2}\, L_{P(MAX)}\, I_{pk(MIN)}^2 \bullet f_s$$

$$= \tfrac{1}{2}\, L_{P(MAX)} \left(\frac{V_{IN(MIN)}}{L_{P(MAX)}}\right)^2 \left(0.45\ T_S\right)^2 f_s$$

$$= \tfrac{1}{2}\ \frac{V_{IN(MIN)}^2}{L_{P(MAX)}} \bullet (0.45\ T_S)^2\, f_s$$

$$\therefore\ L_{P(MAX)} = \tfrac{1}{2}\ \frac{V_{IN(MIN)}^2}{P_{IN(MAX)}} \bullet (0.45\ T_S)^2\, f_s$$

$$= \tfrac{1}{2}\ \frac{(15)^2}{1.25} \bullet (0.45\ T_S)^2\, 10^5 = 182\ \mu H$$

To allow for component tolerances choose a nominal primary inductance of 150 µH. Equation 2 then gives $I_{pk} \approx$ 0.4 A.

Core Selection

The area product method was used to determine the inductor core size. Refer to "Magnetic Core Selection for Transformers and Inductors" by McLyman, for more information on magnetics design methods (Marcel Dekker, Inc., 1982).

$$A_P = \left(\frac{2\ E \bullet 10^4}{B_m \bullet K_u \bullet K_j}\right)^{1.14}$$

where:

E = Core energy storage requirement
B_m = Maximum flux density
K_u = Window utilization factor
K_j = Current density coefficient

$$E = \tfrac{1}{2}\, L_P\, I_{pk}^2$$

Let B_m = 1500, gauss = 0.15 tesla, and K_u = 0.10

$$A_P = \left(\frac{2 \bullet \tfrac{1}{2} \bullet 150 \bullet 10^{-6}\, (0.4)^2\, 10^4}{0.15\ (0.10)\ (433)}\right)^{1.14}$$

$$= 0.0233\ cm^4$$

Since the empirical equation given above applies for the area product of simple one-winding inductors, multiply by 2 for a coupled inductor. All of the secondaries combined will handle the same energy as the primary, and can therefore be allotted equal portions of the window area. The area product requirement is thus:

$$A_P = 2 \bullet 0.0233\ cm^4 = 0.0466\ cm^4$$

The EP-13 core has an area product of 0.049 cm^4, which meets this requirement. Also, this EP core can be tube-loaded for automatic insertion in high volume manufacturing applications, and is available from multiple sources (Siemens, TDK, and Amperex Ferroxcube).

Core A_L Value Determination

The number of primary turns is found from:

$$L = \frac{N_P\, \Phi}{I_{pk}} = \frac{N_P\, B_m\, A_C}{I_{pk}}$$

Limiting the peak flux density to 0.15 Tesla gives:

$$N_P = \frac{L_P I_{pk}}{B_m A_C} = \frac{(150 \bullet 10^{-6})\,(0.4) \bullet 10^4}{(0.15)\,(0.195\ cm^2)}$$

$$= 20.5 \text{ turns} \simeq 21 \text{ turns}$$

This gives the following value for A_L:

$$A_L = \left(\frac{1000}{21}\right)^2 (150 \bullet 10^{-6}) = 340 \text{ mH per } 1000 \text{ turns}$$

Secondary Turns Calculation

The core flux is reset to zero during the off time for each switching cycle. To guarantee discontinuous conduction mode at the maximum load condition, it is necessary to limit the inductance of the secondary windings to some maximum value. Worst case conditions occur at the maximum switching frequency (110 kHz) and maximum A_L value (374 mH/1000 turns for 10 % tolerance). The voltage across N_{S1} during the diode conduction interval is $V_O + V_D = 5.0 + 0.5 = 5.5$ V, and the negative current slope is

$$\frac{di}{dt} = \frac{I_{S1}}{t_{REC}} = \frac{V_O + V_D}{L_{S1}}$$

where I_{S1} is the peak current in the N_{S1} winding, t_{REC} is the conduction time of CR2, and L_{S1} is the inductance of N_{S1}. The rectifier conduction duty ratio is defined as:

$$d_r = \frac{t_{REC}}{T_S}$$

The load current is related to the peak secondary current and duty ratio by the equation:

$$I_{S1} = \frac{2\,S\,I_O}{d_r}$$

Combining these equations solves for the rectifier conduction duty ratio in terms of load current, inductance, and output voltage.

$$d_r = \sqrt{\frac{2 \bullet I_O \bullet L_{S1}}{(V_O + V_D) \bullet T_S}}$$

Setting the duty ratio < 0.45 gives:

$$d_r = \sqrt{\frac{2\,(0.167) \bullet L_{S1}}{5.5\,(9.09)\,10^{-6}}} \leq 0.45$$

Therefore, $L_{S1} < 30.3$ µH. Since $AL_{(MAX)} = 374$ mH/1000 turns,

$$L_{S1} = \left(\frac{N_{S1}}{1000}\right)^2 \bullet (0.374) \leq 30.3\ \mu H$$

$$\therefore \quad N_{S1} \leq 9 \text{ turns}$$

Use $N_{S1} = N_{S2} = 8$ turns:

$$N_{S3} = (10\ V + 0.7\ V)\ \frac{N_{S1}}{5.5\ V}$$

$$= 15.6 \text{ turns} \simeq 16 \text{ turns}$$

Winding Order

The primary winding (1-2) is placed first over the bobbin using one strand of AWG31 magnet wire (21 turns). The highest current secondary (3-4) is wound over the primary using two strands of AWG31 (8 turns). The 10 V sense winding (7-8) is put down next, using one strand of AWG36 (16 turns). The −5 V output (5-6) is wound last using one strand of AWG31 wire (8 turns).

Appendix B: Si9100 Flyback Converter Parts List

U1	Si9100
L1	Inductor, 100 µH @ 75 mA dc
L2	Coupled Inductor, GFS Mfg. # 85-787-4*
C1	20 µF, 100 V, Aluminum Electrolytic, Sprague # 30D+TE1409
C2, C3, C6, C8	0.1 µF ceramic
C4	0.022 µF ceramic
C7	100 µF, 10 V, tantalum, Sprague # 196D107X9010P
C9	20 µF, 10 V, tantalum, Sprague # 196D226X9010J
C5	1 µF, 50 V, WIMA MKS2
CR1	1N4148
CR2, CR3	1N5819, Schottky rectifier
R1	390 kΩ, ¼ W Carbon
R2	1 Ω, ½ W Carbon
R3	150 kΩ, ¼ W Carbon
R4	240 kΩ, ¼ W Carbon
R5	18 kΩ, ¼ W Carbon
R6	12 kΩ, ¼ W Carbon

* GFS Manufacturing Company, 21 Crosby Road, Dover, NH, USA 03820-1409